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Nevill

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[54] **INTEROPERABILITY WITH MULTIPLE INSTRUCTION SETS**

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[*] Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

This patent is subject to a terminal disclaimer.

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Related U.S. Application Data

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[30] **Foreign Application Priority Data**

Jun. 10, 1994 [GB] United Kingdom 9411670

[51] **Int. Cl.**[7] **G06F 9/30**

[52] **U.S. Cl.** **395/385**; 395/386

[58] **Field of Search** 395/384, 385, 395/386

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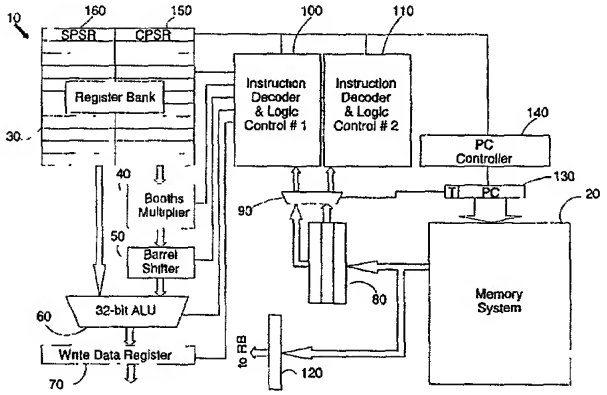
[57] **ABSTRACT**

Data processing apparatus comprising: a processor core having means for executing successive program instruction words of a predetermined plurality of instruction sets; a data memory for storing program instruction words to be executed; a program counter register for indicating the address of a next program instruction word in the data memory; means for modifying the contents of the program counter register in response to a current program instruction word; and control means, responsive to one or more predetermined indicator bits of the program counter register, for controlling the processor core to execute program instruction words of a current instruction set selected from the predetermined plurality of instruction sets and specified by the state of the one or more indicator bits of the program counter register.

14 Claims, 3 Drawing Sheets



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